

AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1 1. (Currently amended) A computerized method for determining a solution
2 to a set of constraints associated with a circuit design, comprising:
3 generating a graph data structure representation for the set of constraints,
4 comprising one or more nodes, each node having an associated range;
5 identifying a first plurality of bit-slice constraint nodes, each selecting
6 from a range of bits of a first variable;
7 converting the first plurality of bit-slice constraint nodes into a second
8 plurality of bit-slice constraints, wherein none of the bit-slice constraints, of the
9 second plurality of bit-slice constraints, select a range of bits that overlaps with a
10 range of bits selected by any other of the bit-slice constraints;
11 generating a value for the first variable that satisfies the second plurality of
12 bit-slice constraints; and
13 displaying the value to a circuit designer to facilitate implementing the
14 circuit design.

1 2. (Original) The method of claim 1, wherein the step of converting
2 comprises:
3 indicating, in relation to the first variable, two marking bits for each node
4 of the first plurality of bit-slice constraint nodes.

1 3. (Original) The method of claim 2, wherein the step of converting
2 comprises:
3 identifying a bit range, of the second plurality of bit-slice constraints, as
4 being denoted by a first marking bit and a second marking bit, wherein a third
5 marking bit is not in-between the first marking bit and the second marking bit.

1 4. (Original) The method of claim 1, wherein the step of generating
2 comprises:
3 selecting a value from a range determined for each bit-slice constraint of
4 the second plurality of bit-slice constraints.

1 5. (Original) The method of claim 4, wherein the step of generating
2 comprises:
3 concatenating each value selected from the range determined for each
4 bit-slice constraint of the second plurality of bit-slice constraints.

1 6. (Currently amended) A computerized method for evaluating bit-slice
2 nodes in a word-level network, comprising:
3 generating a graph data structure representation for a set of constraints
4 associated with a circuit design, comprising one or more nodes, each node having
5 an associated range;
6 identifying a first plurality of bit-slice nodes, each selecting from a range
7 of bits of a first operand;
8 converting the first plurality of bit-slice nodes into a second plurality of
9 bit-slice selectors, wherein none of the bit-slice selectors, of the second plurality
10 of bit-slice selectors, select a range of bits that overlaps with a range of bits
11 selected by any other of the bit-slice selectors;

12 determining a first range of values, for the first operand, that satisfies the
13 second plurality of bit-slice selectors; and
14 displaying the first range of values to a circuit designer to facilitate
15 implementing the circuit design.

1 7. (Original) A computer program product comprising:
2 a computer usable medium having computer readable code embodied
3 therein for evaluating bit-slice nodes in a word-level network, the computer
4 program product including:
5 computer readable program code devices configured to cause a computer
6 to effect generating a graph data structure representation, comprising one or more
7 nodes, each node having an associated range;
8 computer readable program code devices configured to cause a computer
9 to effect identifying a first plurality of bit-slice nodes, each selecting from a range
10 of bits of a first operand;
11 computer readable program code devices configured to cause a computer
12 to effect converting the first plurality of bit-slice nodes into a second plurality of
13 bit-slice selectors, wherein none of the bit-slice selectors, of the second plurality
14 of bit-slice selectors, select a range of bits that overlaps with a range of bits
15 selected by any other of the bit-slice selectors;
16 computer readable program code devices configured to cause a computer
17 to effect determining a first range of values, for the first operand, that satisfies the
18 second plurality of bit-slice selectors.

1 8. (Currently amended) A computer-readable storage medium ~~An~~
2 ~~electromagnetic waveform~~ comprising a computer program, the computer
3 program for evaluating bit-slice nodes in a word-level network, the computer

4 program comprising the following steps when executed by a data processing
5 system:
6 generating a graph data structure representation, comprising one or more
7 nodes, each node having an associated range;
8 identifying a first plurality of bit-slice nodes, each selecting from a range
9 of bits of a first operand;
10 converting the first plurality of bit-slice nodes into a second plurality of
11 bit-slice selectors, wherein none of the bit-slice selectors, of the second plurality
12 of bit-slice selectors, select a range of bits that overlaps with a range of bits
13 selected by any other of the bit-slice selectors;
14 determining a first range of values, for the first operand, that satisfies the
15 second plurality of bit-slice selectors.